What is claimed is:

1. A method for temperature compensation for a memory cell with temperature-dependent behavior, the method comprising:

(a) generating at least one of a first temperature-dependent reference voltage comprising a negative temperature coefficient and a second temperature-dependent reference voltage comprising a positive temperature coefficient;

(b) generating one of a wordline voltage and a bitline voltage from one of the at least one of the first and second temperature-dependent reference voltages;

(c) generating the other of the wordline and bitline voltages; and

(d) applying the wordline and bitline voltages across a memory cell.

2. The invention of Claim 1, wherein (a) comprises generating both the first and second temperature-dependent reference voltages, and wherein (c) comprises generating the other of the wordline and bitline voltages from the other of the at least one of the first and second temperature-dependent reference voltages.

3. The method of Claim 1, wherein (d) is performed during a write operation.

4. The method of Claim 1, wherein (d) is performed during a read operation.

5. The method of Claim 1, wherein the temperature coefficient(s) of the at least one of the first and second temperature-dependent reference voltages are chosen such that a voltage across the memory cell comprises a negative temperature coefficient.

6. The method of Claim 1, wherein the memory cell comprises a write-once memory cell.

7. The method of Claim 1, wherein the memory cell comprises a write-many memory cell.

8. The method of Claim 1, wherein the memory cell is part of a two-dimensional memory array.

9. The method of Claim 1, wherein the memory cell is part of a three-dimensional memory array.

10. The method of Claim 1, wherein the memory cell comprises a non-volatile memory cell.

11. A system for temperature compensation for a memory cell with temperature-dependent behavior, the system comprising:

a first temperature-dependent reference voltage source operative to generate a first temperature-dependent reference voltage comprising a negative temperature coefficient;

a second temperature-dependent reference voltage source operative to generate a second temperature-dependent reference voltage comprising a positive temperature coefficient;

a wordline voltage regulator operative to generate a wordline voltage from one of the first and second temperature-dependent reference voltages;

a bitline voltage regulator operative to generate a bitline voltage from the other of the first and second temperature-dependent reference voltages; and

a memory cell coupled with the wordline and bitline voltage regulators.

12. The system of Claim 11 further comprising:

a temperature-dependent current source operative to generate a first reference current with a negative temperature coefficient; and

a temperature-independent current source operative to generate a second reference current;

wherein the first and second temperature-dependent reference voltage sources generate the first and second temperature-dependent reference voltages, respectively, from the first and second reference currents.

13. The system of Claim 11, wherein at least one of the temperature-dependent current source, the first temperature-dependent reference voltage source, and the second temperature-dependent reference voltage source comprises a temperature-dependent resistor.

14. The system of Claim 11, wherein at least one of the temperature-dependent current source, the first temperature-dependent reference voltage source, and the second temperature-dependent reference voltage source comprises a temperature-independent resistor.

15. The system of Claim 11, wherein the temperature coefficients of the first and second reference voltages are chosen such that a voltage across the memory cell comprises a negative temperature coefficient.

16. The system of Claim 11, wherein the memory cell comprises a write-once memory cell.

17. The system of Claim 11, wherein the memory cell comprises a write-many memory cell.

18. The system of Claim 11, wherein the memory cell is part of a two-dimensional memory array.

19. The system of Claim 11, wherein the memory cell is part of a three-dimensional memory array.

20. The system of Claim 11, wherein the memory cell comprises a non-volatile memory cell.

21. A system for sensing a memory cell comprising temperature-dependent behavior, the system comprising:

a memory cell comprising temperature-dependent behavior;

a current sensing amplifier coupled with the memory cell; and

a set of memory cells coupled with the current sensing amplifier, the set of memory cells generating a current reference when a voltage is applied to the set of memory cells;

wherein the current sensing amplifier compares the current reference to current sensed back from the memory cell during a read operation to determine whether the memory cell is programmed.

22. The system of Claim 21 further comprising a programmable mirror interposed between the set of memory cells and the current sensing amplifier.

23. The system of Claim 21, wherein the memory cell comprises a write-once memory cell.

24. The system of Claim 21, wherein the memory cell comprises a write-many memory cell.

25. The system of Claim 21, wherein the memory cell is part of a two-dimensional memory array.

26. The system of Claim 21, wherein the memory cell is part of a three-dimensional memory array.

27. The system of Claim 21, wherein the memory cell comprises a non-volatile memory cell.

28. A system for sensing a memory cell comprising temperature-dependent behavior, the system comprising:

a memory cell comprising temperature-dependent behavior;

a current sensing amplifier coupled with the memory cell; and

a temperature-dependent reference current source coupled with the current sensing amplifier, the temperature-dependent reference current source operative to generate a temperature-dependent reference current comprising a positive temperature coefficient;

wherein the current sensing amplifier compares the temperature-dependent reference current to current sensed back from the memory cell during a read operation to determine whether the memory cell is programmed.

29. The system of Claim 28 further comprising:

a second temperature-dependent current source, the second temperature-dependent current source operative to generate a reference current with a negative temperature coefficient; and

a temperature-independent current source operative to generate a temperature-independent reference current;

wherein the temperature-dependent reference current source generates the temperature-dependent reference current from the reference current generated by the second temperature-dependent current source and the temperature-independent reference current.

30. The system of Claim 28, wherein the memory cell comprises a write-once memory cell.

31. The system of Claim 28, wherein the memory cell comprises a write-many memory cell.

32. The system of Claim 28, wherein the memory cell is part of a two-dimensional memory array.

33. The system of Claim 28, wherein the memory cell is part of a three-dimensional memory array.

34. The system of Claim 28, wherein the memory cell comprises a non-volatile memory cell.